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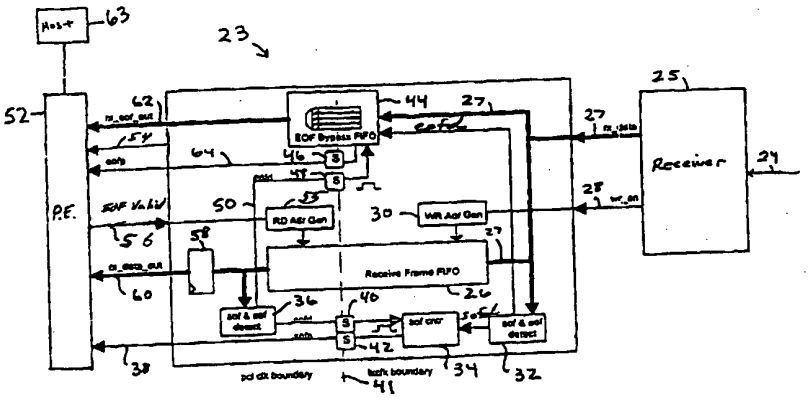

(57) Abstract

A method and apparatus for processing and transferring of frames of data in a computer data link. A receive frame FIFO buffer (26) stores each frame received from a data receiver (25) over a serial data channel (24). The data frames each have at least a start of frame (SOF) word, a payload, and an end of frame (EOF) word. An EOF status word is generated in part from information in each EOF word. When an EOF status word is generated, the EOF status word is stored in a separate end of frame bypass FIFO (44). At an appropriate time, the receive frame FIFO buffer (26) transmits to a protocol engine (52), beginning with the SOF word. At the same time, the EOF status word is transmitted out of the end of frame bypass FIFO (44). As a result, the end of frame status information is available to the protocol engine (52) at the same time as the SOF word. This avoids any delay in receiving status information relating to the frame. In the preferred embodiment, the data channel is a Fibre Channel link.

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RECEIVE FRAME FIFO WITH END OF FRAME BYPASS

BACKGROUND OF THE INVENTION

1. *Field of the Invention*

This invention relates to transferring of data in computer networks, and more particularly to processing of a frame of data upon transfer across a network boundary.

2. *Description of Related Art*

The number of computers and peripherals has mushroomed in recent years. This has created a need for improved methods of interconnecting these devices. A wide variety of networking paradigms have been developed to enable different kinds of computers and peripheral components to communicate with each other.

There exists a bottleneck in the speed with which data can be exchanged along such networks. This is not surprising because increases in network architecture speeds have not kept pace with faster computer processing speeds. The processing power of computer chips has historically doubled about every 18 months, creating increasingly powerful machines and bandwith hungry applications. It has been estimated that one megabit per second of input/output is generally required per "MIPS" (millions of instructions per second) of processing power. With CPUs now easily exceeding 200 MIPS, it is difficult for networks to keep up with these faster speeds.

Area-wide networks and channels are two approaches that have been developed for computer network architectures. Traditional networks (*e.g.*, LAN's and WAN's) offer a great deal of flexibility and relatively large distance capabilities. Channels, such as Enterprise System Connection (ESCON) and Small Computer System Interface (SCSI), have been developed for high performance and high reliability. Channels typically use dedicated short-distance connections between computers or between computers and peripherals.

Features of both channels and networks have been incorporated into a new network standard known as "Fibre Channel". Fibre Channel systems combine the speed and reliability of channels with the flexibility and connectivity of networks. Fibre Channel products currently can run at very high data rates, such as 266 or 1062 Mbps. These speeds are sufficient to handle quite demanding applications such as uncompressed, full motion, high-quality video.

There are generally three ways to deploy Fibre Channel: simple point-to-point connections; arbitrated loops; and switched fabrics. The simplest topology is the point-to-point configuration, which simply connects any two Fibre Channel systems directly. Arbitrated loops are Fibre Channel ring connections that provide shared access to bandwidth via arbitration. Switched Fibre Channel networks, called "fabrics", yield the highest performance by leveraging the benefits of cross-point switching.

The Fibre Channel fabric works something like a traditional phone system. The fabric can connect varied devices such as work stations, PCs, servers, routers, mainframes, and storage devices that have Fibre Channel interface ports. Each such device can have an origination port that "calls" the fabric by entering the address of a destination port in a frame header. The Fibre Channel specification defines the structure of this frame. (This frame structure raises data transfer issues that will be discussed below and addressed by the present invention). The Fibre Channel fabric does all the work of setting up the desired connection, hence the frame originator does not need to be concerned with complex routing algorithms. There are no complicated permanent virtual circuits (PVCs) to set up. Fibre Channel fabrics can handle more than 16 million addresses and so are capable of accommodating very large networks. The fabric can be enlarged by simply adding ports. The aggregate data rate of a fully configured Fibre Channel network can be in the tera-bit-per-second range.

Each of the three basic types of Fibre Channel connections are shown in FIGURE 1, which shows a number of ways of using Fibre Channel technology. In particular, point-to-point connections 10 are shown connecting mainframes to each other. A Fibre Channel arbitrated loop 11 is shown connecting disk storage units. A Fibre Channel switch fabric 12 connects

work stations 13, mainframes 14, servers 15, disk drives 16 and local area networks (LANs) 17. Such LANs include, for example, Ethernet, Token Ring and FDDI networks.

An ANSI specification (X3.230-1994) defines the Fibre Channel network. This specification distributes Fibre Channel functions among five layers. As shown in FIGURE 2, the five functional layers of the Fibre Channel are: FC-0 - the physical media layer; FC-1 - the coding and encoding layer; FC-2 - the actual transport mechanism, including the framing protocol and flow control between nodes; FC-3 - the common services layer; and FC-4 - the upper layer protocol.

While the Fibre Channel operates at relatively high speed, it would be desirable to increase speeds further to meet the needs of faster processors. One way to do this would be to eliminate or reduce delays that occur at interface points. One such delay occurs during the transfer of a frame from the FC-1 layer to the FC-2 layer. At this interface, devices linked by a Fibre Channel data link receive Fibre Channel frames serially. A Fibre Channel receiver unit typically decodes and parallelizes the received serial link data into four-byte words. The receiver assembles the data into frames within a buffer memory, called the receive frame FIFO (first in-first out) buffer, in the FC-1 layer. In order for a frame to be processed by the next layer, the FC-2 layer, a protocol engine needs access to status information contained within an end of frame (EOF) word in the frame stored in the receive frame FIFO buffer. However, the EOF status information is not available from the receive frame FIFO until the frame payload has been read out of the receive frame FIFO. This creates a processing delay while the frame payload unloads and the protocol engine waits to get the End of Frame status information. The delay is dependent on the size of the frame payload (which can be as much as 2112 bytes), and the speed at which the FIFO can be unloaded. For a 2 Kbyte payload (the most normal case) and a protocol engine running at 33 MHz the delay in accessing the EOF status word will be 15.36 μs.

More particularly, FIGURE 3 shows an example of a receive frame FIFO module 18 in accordance with the prior art. The receive frame FIFO module 18 includes a receive frame

FIFO buffer 19. The receive frame FIFO module 18 performs the function of receiving and preparing a data frame along a serial link 20 for processing by a protocol engine 21. The protocol engine 21 serves several functions, including (1) queuing up a host command to write the data in the frame into host memory through direct memory access (DMA); (2) validating the header to ensure that the frame is the next logical header that should be received; and (3) determining whether the frame is defective or not. The receive frame FIFO module 18 in FIGURE 3 represents one component of a Fibre Channel network, or other network having similar processing functions.

The serial data received on data link 20 is sent to a receiver 22. The receiver 22, including an FC-0 layer transceiver and the FC-1 layer port logic (NL-Port), decodes and parallelizes the incoming serial data into four-byte words. The receiver 22 then assembles these words into frames. Frames generally will comprise three portions, a preamble, a data or "payload" portion, and a trailer portion. In a Fibre Channel data link, for example, the Fibre Channel frame consists of a start of frame (SOF) word (four bytes); a data portion comprising a frame header (six bytes), between zero and 2112 payload bytes, and a cyclical redundancy check (CRC) word (4 bytes); and an end of frame (EOF) word (4 bytes). The frame header is used to control link applications, control device protocol transfers, and detect missing or out of order frames. The CRC word indicates whether there is a problem in the transmission, such as a data corruption, or whether some part of the frame was dropped during transmission. The receiver checks the CRC word for each frame received and adds a resulting "good/bad" CRC status indicator to other status information bits within an EOF status word generated in part from the EOF word, in known fashion. The EOF status word also contains the length of the frame payload. The receiver 22 assembles these words into frames by writing the frames into the receive frame FIFO buffer 19.

After processing by the receiver 22, the frame needs to be processed into the next layer of protocol checking by the protocol engine 21. For example, in the Fibre Channel data link this next layer is the FC-2 layer, shown in FIGURE 2. However, before the frame can be processed, the protocol engine 21 needs access to the SOF word, the frame header, and the

status information within the EOF status word. The protocol engine 21 needs to know the length of the frame before it can make the transfer. It must queue up a DMA operation which matches the size of the frame. The protocol engine 21 also needs the CRC status before the protocol engine 21 transfers the frame to the host; validating the frame at this stage is preferable to dealing with a defective frame after it has been sent to the host.

A problem with the prior art is that the EOF status information is not available from the receive frame FIFO module 18 until the frame payload has been read out of the receive frame FIFO memory 19. The result is a processing delay while the protocol engine 21 unloads the frame payload in order to gain access to the EOF status word status information.

In view of the foregoing, it is an object of the invention to increase data transfer processing speeds in high speed networks such as Fibre Channel. It is also an object of the invention to provide a way to avoid the processing delays incurred when a protocol engine waits to unload frame payload data until the protocol engine obtains End of Frame data. It is another object of the invention to provide the protocol engine with early access to the status information within an EOF status word. It is another object of the invention to provide a Fibre Channel receive frame FIFO which can speed up the processing of a data frame by the protocol engine. The present invention meets these needs.

SUMMARY OF THE INVENTION

The invention is directed to processing and transferring frames of data in a computer data link. According to one aspect of the invention, a receive frame FIFO buffer stores each frame received from a data receiver over a serial data channel. The data frames that are stored in the receive frame FIFO buffer each have at least a start of frame (SOF) word, a data portion including a header and a payload, and an end of frame (EOF) word. An EOF status word is generated in part from information in each EOF word. When an EOF status word is generated, the EOF status word is stored in a separate end of frame bypass FIFO.

At an appropriate time, the receive frame FIFO buffer transmits to a protocol engine, beginning with the SOF word. At the same time, the EOF status word is transmitted out of the end of frame bypass FIFO. As a result, the end of frame status information is available to the protocol engine at the same time as the SOF word. This avoids any delay in receiving status information relating to the frame. In the preferred embodiment, the data channel is a Fibre Channel link.

The details of the preferred embodiment of the present invention are set forth in the accompanying drawings and the description below. Once the details of the invention are known, numerous additional innovations and changes will become obvious to one skilled in the art.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGURE 1 is a block diagram of a prior art complex computer network utilizing Fibre Channel technology.

FIGURE 2 is a diagram of the five functional layers of the prior art Fibre Channel standard.

FIGURE 3 is a simplified block diagram of a receive frame FIFO in accordance with the prior art.

FIGURE 4 is a diagram of a typical prior art Fibre Channel frame of data.

FIGURE 5 is a block diagram of a receive frame buffer FIFO module having an End of Frame bypass FIFO in accordance with the present invention.

FIGURE 6 is a flowchart of the method of processing a data frame in accordance with the present invention.

Like reference numbers and designations in the various drawings refer to like elements.

DETAILED DESCRIPTION OF THE INVENTION

Throughout this description, the preferred embodiment and examples shown should be considered as exemplars, rather than as limitations on the present invention.

The present invention avoids any time delay in processing frames by making the EOF status word available to a protocol engine at the same time that the protocol engine reads the Start of Frame (SOF) word and frame header from a receive frame FIFO module. Hence, the protocol engine does not have to wait for a lengthy frame payload (up to 528 4-byte words) to be unloaded. In the preferred embodiment of the present invention, the receive frame FIFO is adapted to operate within the Fibre Channel data link. However, the teachings of the present invention may be readily adapted to other kinds of data links where similar processing delays are encountered.

FIGURE 5 shows a preferred embodiment of a receive frame FIFO system 23 in accordance with the invention. Serial data is received along a Fibre Channel data link 24 and enters a receiver unit 25, which comprises a conventional Fibre Channel data link receiver unit. For example, receiver unit 25 may comprise a receiver unit such as the one shown in FIGURE 3.

The data that receiver 25 acquires from the Fibre Channel link 24 consists of Fibre Channel frames such as the one shown in FIGURE 4. The receiver 25 decodes and parallelizes this serial data into four-byte words. The receiver 25 also generates and checks the cyclical redundancy check (CRC) word for each frame received and the resulting good/bad CRC status is added to other status information bits within the EOF status word. The receiver also adds the length of the frame payload to the EOF status word. The words of the frame are then written into a receive frame FIFO buffer 26 through data line 27, under the control of a write enable signal 28 from the receiver 25. In the illustrated embodiment, the write enable signal 28 causes an address generator 30 to generate addresses for the receive frame FIFO buffer 26.

A first Start of Frame and End of Frame (SOF/EOF) detection unit 32 detects both the SOF word and EOF status words received on data line 27. Upon detection of the SOF word, the first SOF/EOF detection unit 32 sends a signal to an SOF counter unit 34 which is used to count the number of SOF words received. The SOF counter 34 also receives an "sofd" signal from a second SOF/EOF detection unit 36. The purpose of this signal is to decrement the counter as an SOF word is removed from the FIFO. The SOF counter 34 sends an "sofp" output along line 38 which is used to indicate that one or more SOF words are present within the FIFO.

One function of the receive frame FIFO system 23 is to synchronize between two clock frequencies. In this case, the input side is at one clock frequency "Tx clock", while on the output side the system interfaces with a peripheral component interface (PCI) clock frequency. Synchronizers 40, 42, 46 and 48, are used for synchronizing signals passing from one clock frequency side to the other. The clock boundary is the vertical line at 41.

When the EOF status word is detected by the first SOF/EOF detection unit 32, an EOF bypass FIFO 44 is triggered to receive the EOF status word along line 27. In a preferred embodiment, the EOF bypass FIFO comprises a RAM memory. An "eofd" signal 50 from the second SOF/EOF detection unit 36 is used to decrement the count of the number of EOF status words within the EOF bypass FIFO.

A protocol engine 52 receives the receive frame FIFO system 23 output. The protocol engine 52 is similar to a conventional protocol engine 21, as shown in FIGURE 3, except that it is designed so that it can accept SOF words and EOF status words simultaneously. Thus, the protocol engine 52 avoids any delay in waiting for the EOF status word. When the protocol engine 52 is ready to receive a frame, it de-asserts an EOF valid signal 56. The EOF valid signal 56 is sent to the read address generator 55. In response, the frame (beginning with the SOF word) is sent from the receive frame FIFO memory 26 to a register 58, and then to the protocol engine 52. The purpose of register 58 is to capture and hold the output of the FIFO.

The state of the EOF valid signal 56 of the protocol engine 52 indicates the presence or non-presence of an EOF word. De-assertion of the EOF valid signal 56 causes the EOF bypass FIFO 44 to send the EOF status word along data line 62 to the protocol engine 52. Since the EOF status word has been previously received in the bypass FIFO 44, the EOF status word can be sent to the protocol engine 52 at the same time that the SOF word is sent along data line 60. In the preferred embodiment, on subsequent clock cycles the receive frame FIFO 26 transmits the header words to the protocol engine 52 along data line 60, using data line 54 to indicate which header word is present on data line 60.

The protocol engine 52 then can proceed with validating the received frame and preparing for data transfer to a host 63 without incurring the time penalty of unloading the entire frame payload from the receive frame FIFO memory 26 to gain access to the EOF status word. The eofp signal 64 is sent from the EOF bypass FIFO 44 for the purpose of indicating that one or more EOF status words are present within the EOF bypass FIFO, thus indicating the presence of one or more complete frames within the receive frame FIFO.

Referring now to FIGURE 6, a flowchart of a preferred method of the present invention is shown. Initially, a write enable signal is sent from the receiver 25 (block 65). This causes the receiver 25 to write a data frame into the receive frame FIFO memory 26 (block 66). This process continues until an EOF status word is detected (block 67). Once the EOF status word is detected, the system writes the EOF status word into both the EOF bypass FIFO 44 and the receive frame FIFO 26 (block 68). The system then waits for an EOF valid signal from the protocol engine 52 (block 70). When an EOF valid signal is de-asserted (block 70), the system simultaneously writes the SOF word from the receive frame FIFO memory 26 and the EOF status word from the EOF bypass FIFO 44 to the protocol engine 52 (block 72). The protocol engine 52 then validates and processes the received frame (block 74).

In summary, the invention speeds up the transfer of data in networked environments, such as Fibre Channel network systems, by providing end of frame data words simultaneously with start of frame data words to a protocol engine. Hence, the protocol engine does not need to

unload the entire data payload in order to check the CRC status of a frame. Another advantage of the invention is that it avoids a need for additional storage (RAM) for the protocol engine that otherwise would be needed to save the payload data as such data is unloaded from the receive frame FIFO 26, in order to access the EOF status word. Such "double buffering" would degrade system receive performance.

A number of embodiments of the present invention have been described. Nevertheless, it will be understood that various modifications may be made without departing form the spirit and scope of the invention. For example, although the system has been described in the Fibre Channel environment, the teachings of the invention may be utilized in other environments where it is desired to receive data at the end of a frame simultaneously with the beginning of the frame to avoid time delays incurred by waiting for the frame payload data to unload. Accordingly, it is to be understood that the invention is not to be limited by the specific illustrated embodiment, but only by the scope of the appended claims.

CLAIMS

What is claimed is:

1. A method for transferring data in a computer network comprising:
   (a) receiving data frames each having at least a start of frame word, a payload, and an end of frame (EOF) word;
   (b) transmitting each data frame to a receive frame storage unit, beginning with the SOF word;
   (c) generating an EOF status word for each data frame at least in part from the EOF word of such data frame;
   (d) storing each EOF status word into an end of frame bypass storage unit; and
   (e) transmitting the SOF word from the receive frame storage unit and the EOF status word from the end of frame bypass storage unit to a protocol engine, whereby the protocol engine receives the SOF word and the EOF status word prior to receiving the payload.

2. A method according to claim 1, wherein the end of frame bypass storage unit is a first in first out (FIFO) memory.

3. A method according to claim 1, comprising the step of validating the received data frame based on information in the EOF status word.

4. A method according to claim 1, wherein the data frame is a Fibre Channel data frame.

5. A method according to claim 1, comprising the step of synchronizing the received data frame with the data frame transmitted to the protocol engine.

6. A system for transferring data between components in a computer system comprising:
   (a) a data path for coupling data frames each having at least a start of frame word, a payload, and an end of frame (EOF) word;
   (b) a receiver for processing said data frame, wherein the receiver transmits each data frame to a receive frame storage unit;
   (c) an end of frame bypass storage unit;
   (d) means for generating an EOF status word for each data frame at least in part from the EOF word of such data frame;
   (e) means for storing each EOF status word into the end of frame bypass storage unit;
   (f) a protocol engine coupled to the receive frame storage unit and to the end of frame bypass storage unit; and
   (g) means for transmitting the SOF word from the receive frame storage unit and the EOF status word from the end of frame bypass storage unit to the protocol engine prior to transmitting the payload words.

7. A system according to claim 6, wherein the end of frame bypass storage unit is a first in first out (FIFO) memory.

8. A system according to claim 6, wherein the end of frame bypass storage unit includes a RAM memory.

9. A system according to claim 6, wherein each data frame is a Fibre Channel data frame.

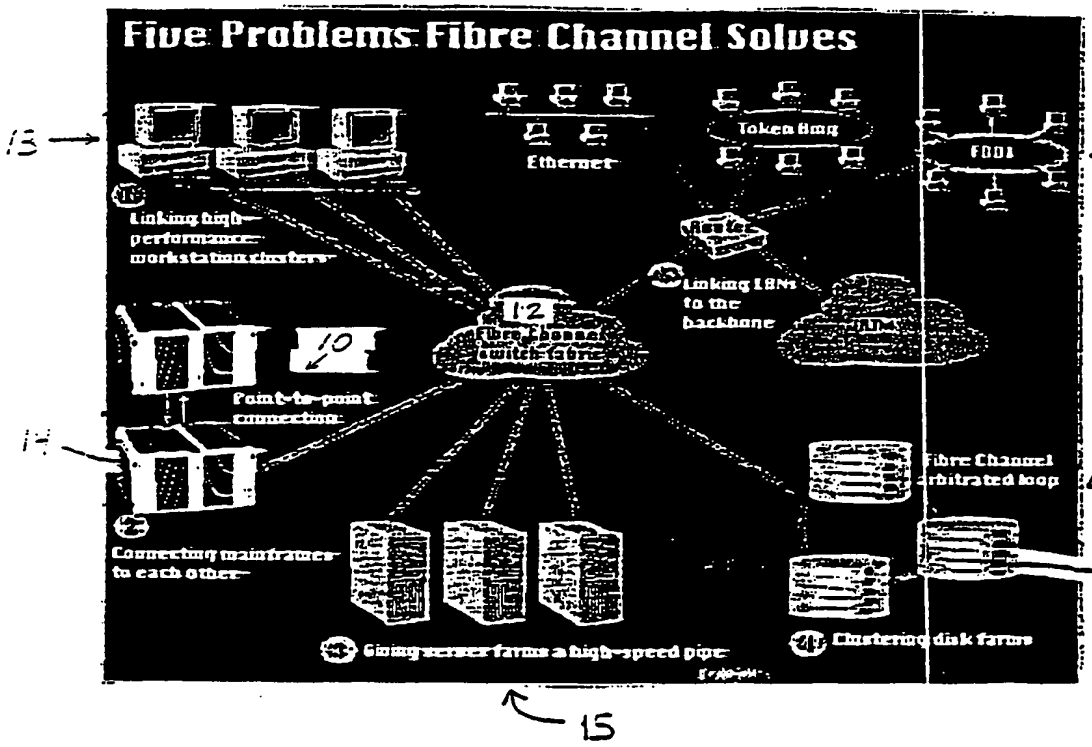

FIG 1
(Prior Art)

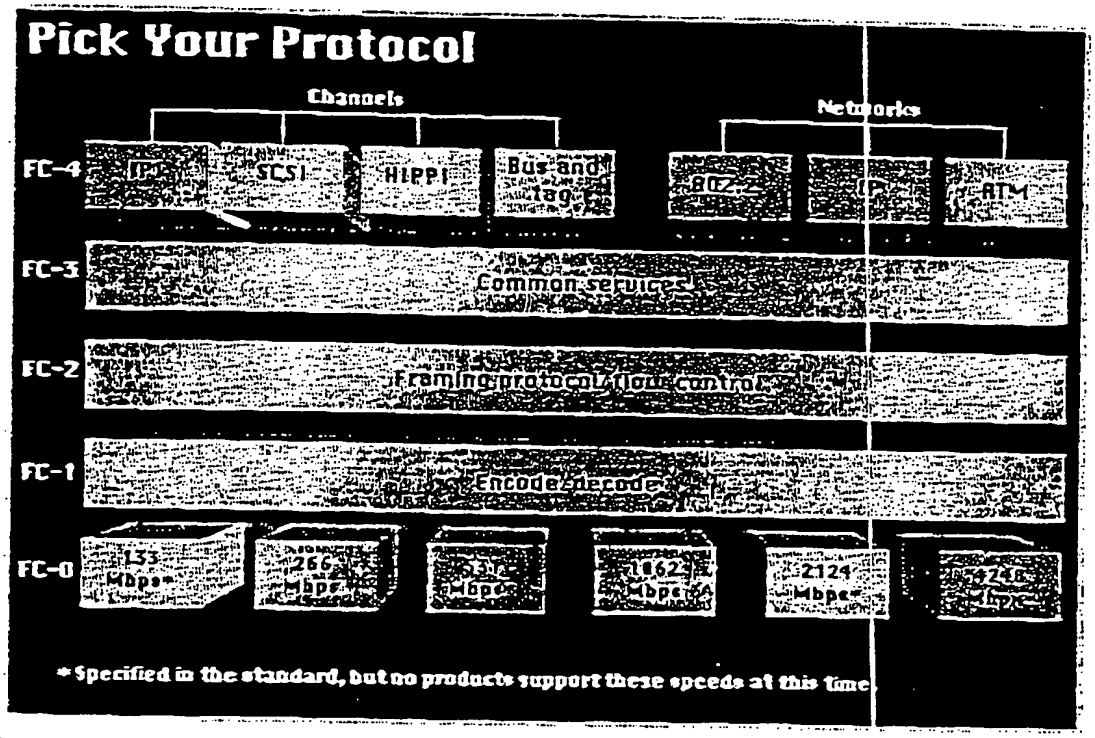

FIG 2
(Prior Art)

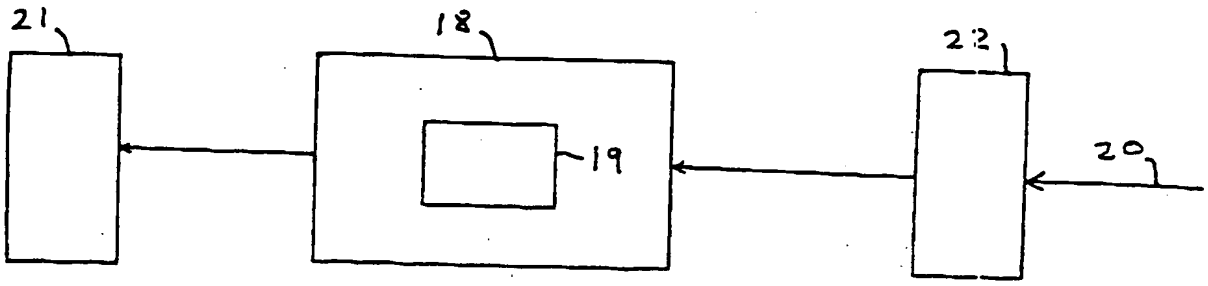

FIG 3 (prior art)

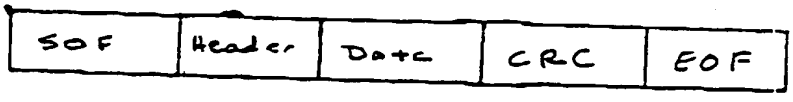

FIG 4
(Prior Art)

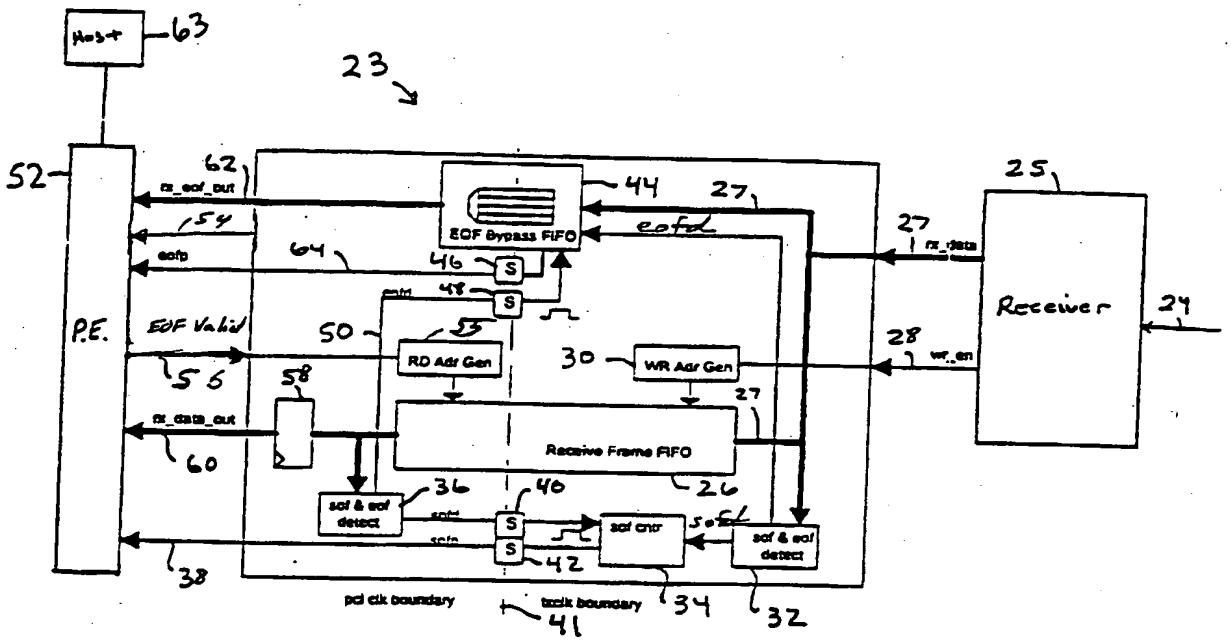

FIG 5

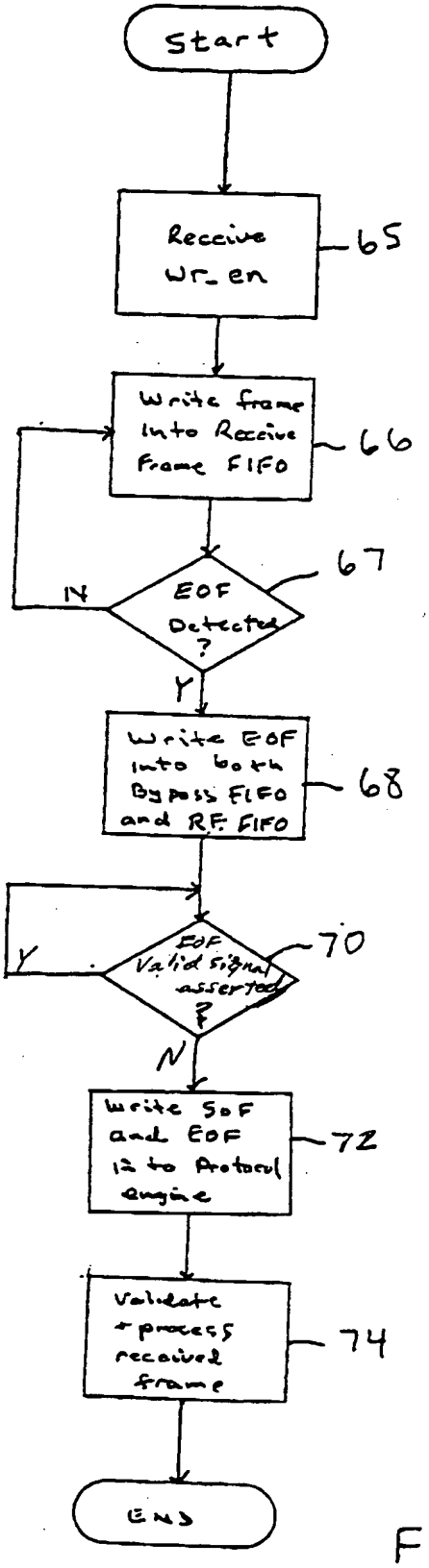

FIG 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/19966

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :G06F 13/00
US CL :395/200.8, 872

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 395/200.8, 872

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

aps

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 5,151,999 A (MARZUCCO et al.) 29 September 1992, abstract col.2-3	1-3,6-8 --- 4-5,9
Y	US 5,490,007 A (BENNETT et al.) 06 February 1996, abstract	4-5,9

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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